

FIG. 3

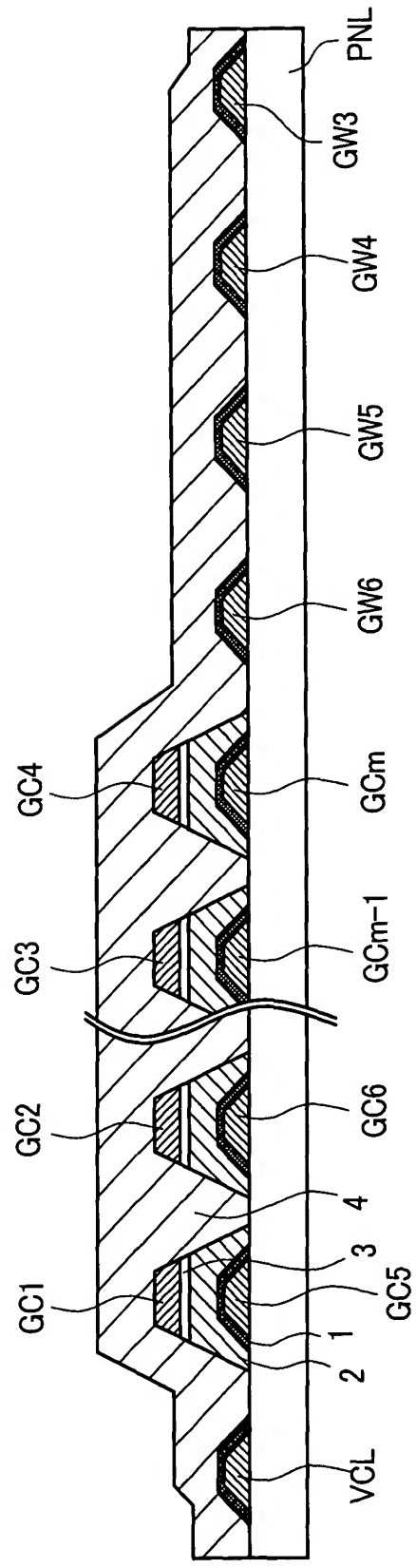


FIG. 4

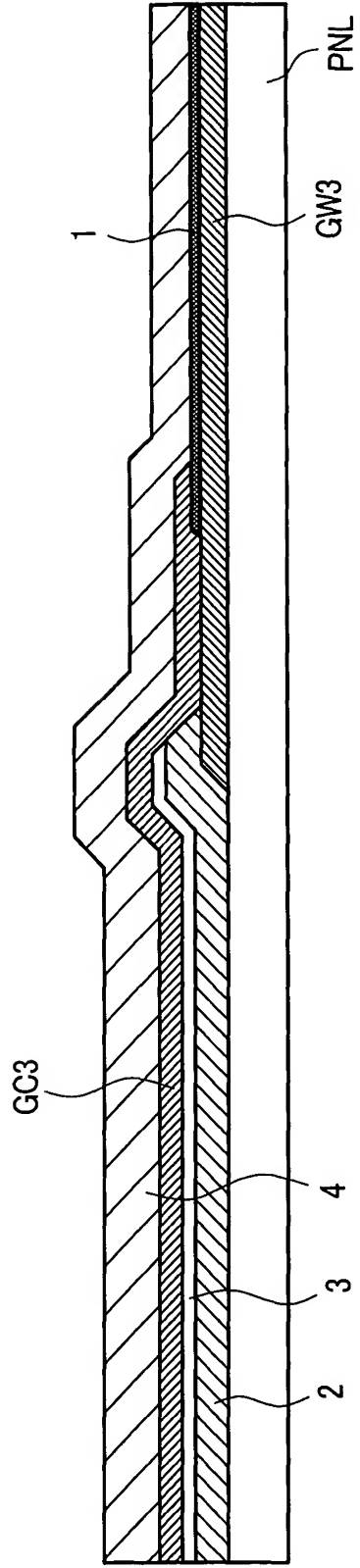


FIG. 5

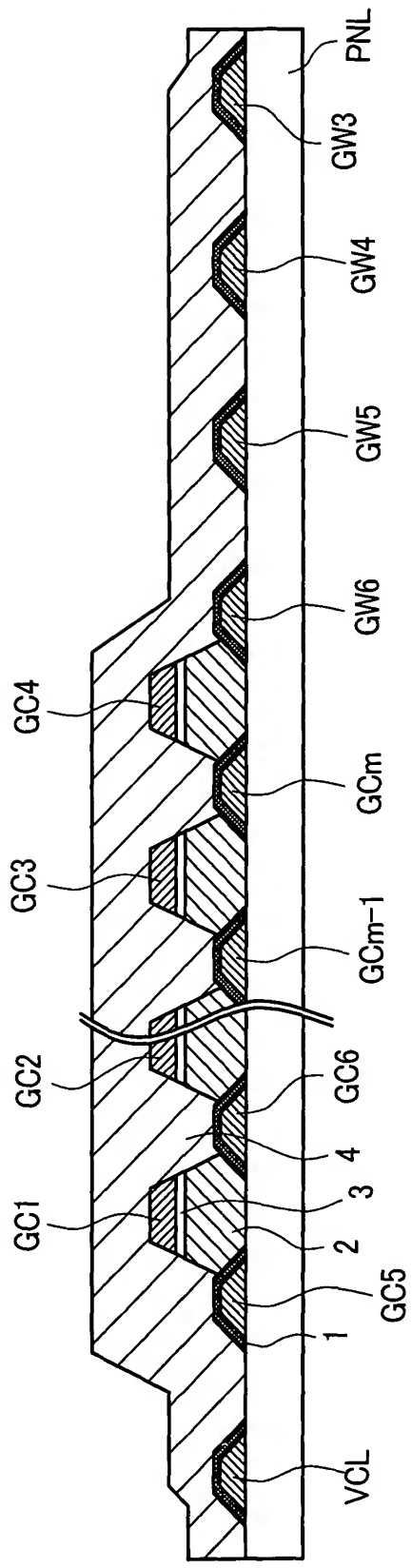


FIG. 6

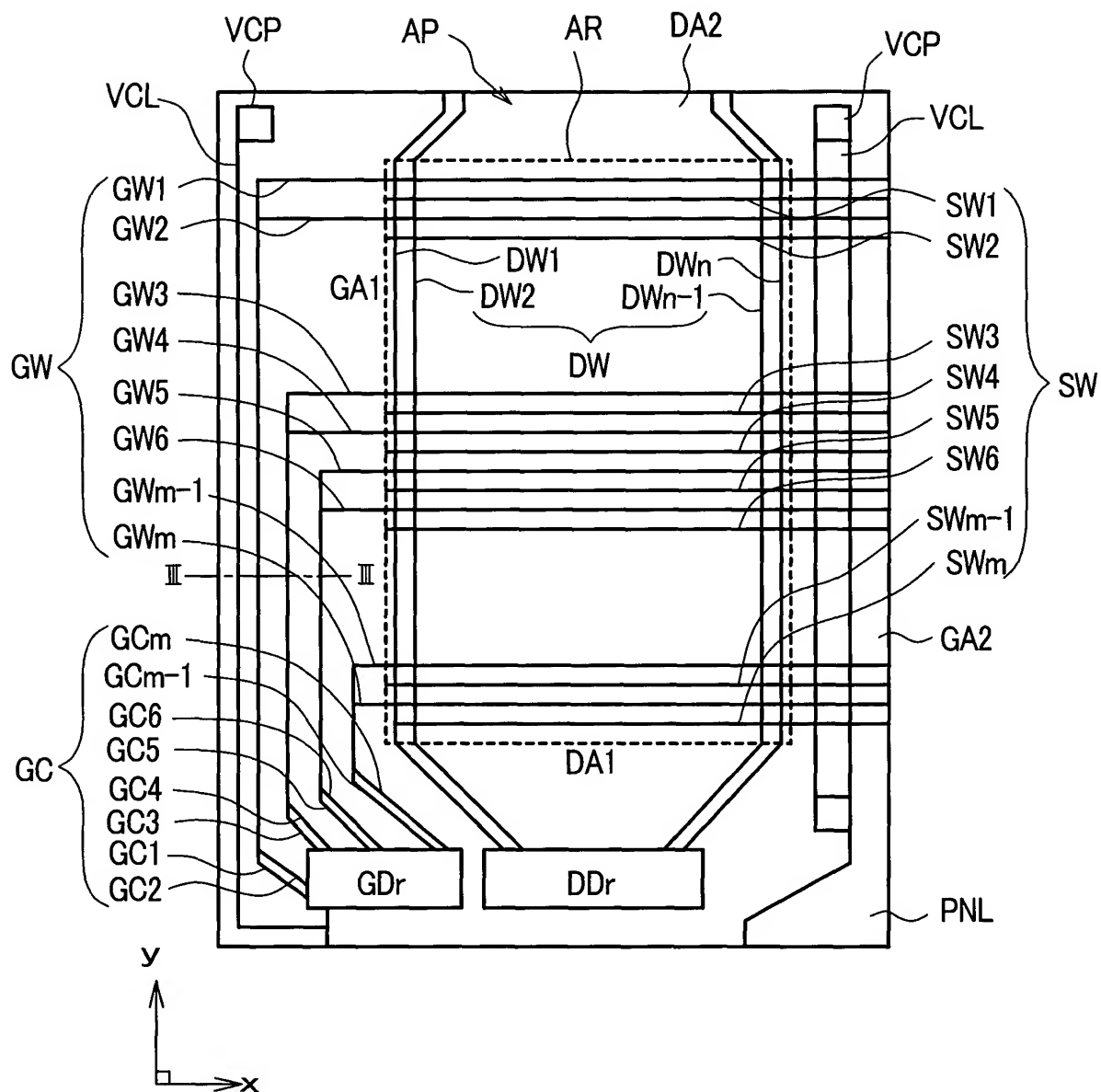


FIG. 7

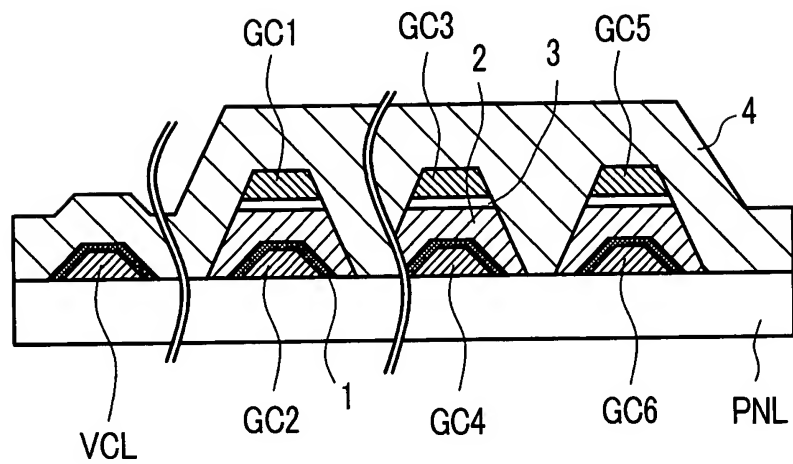


FIG. 8

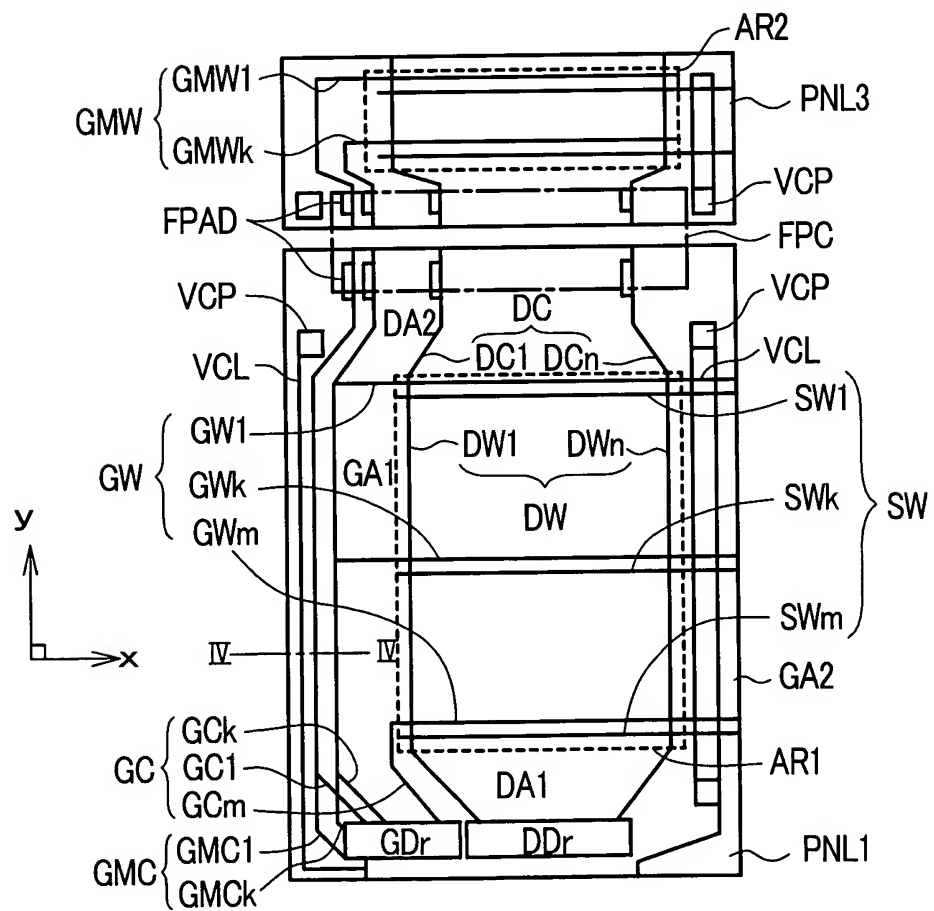


FIG. 9

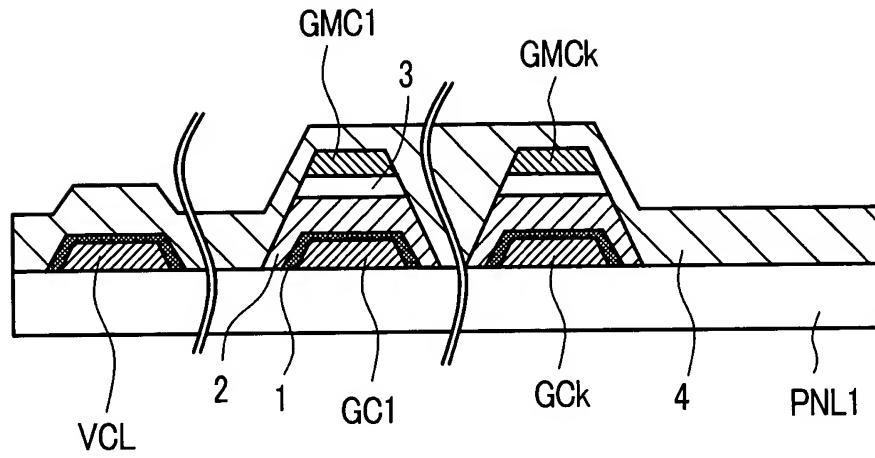
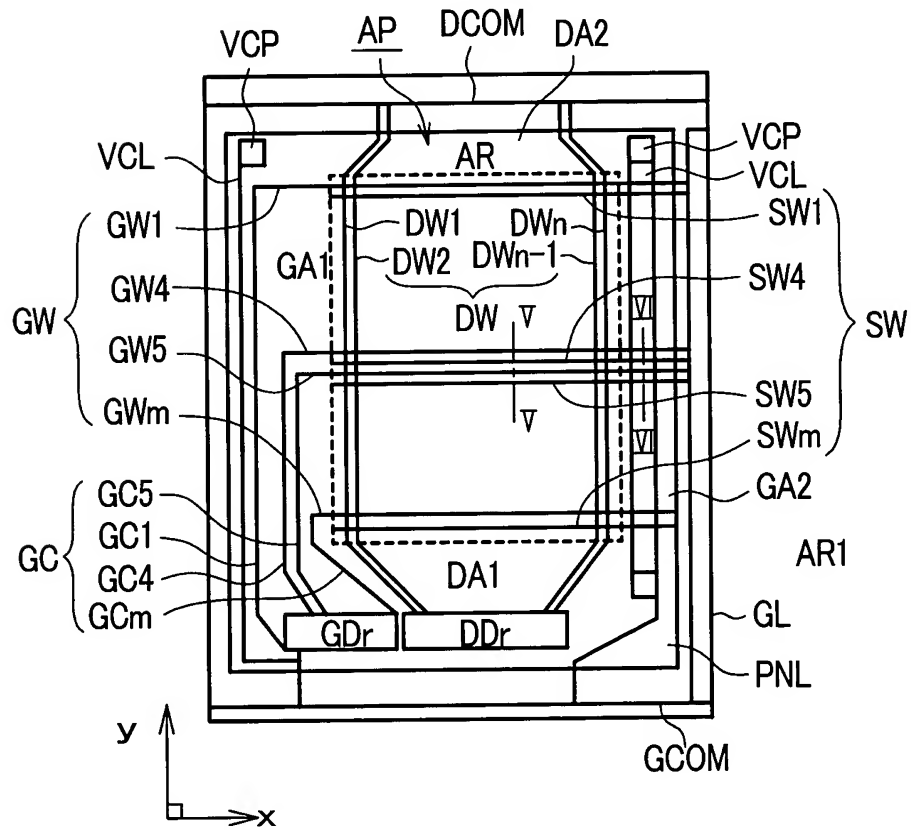
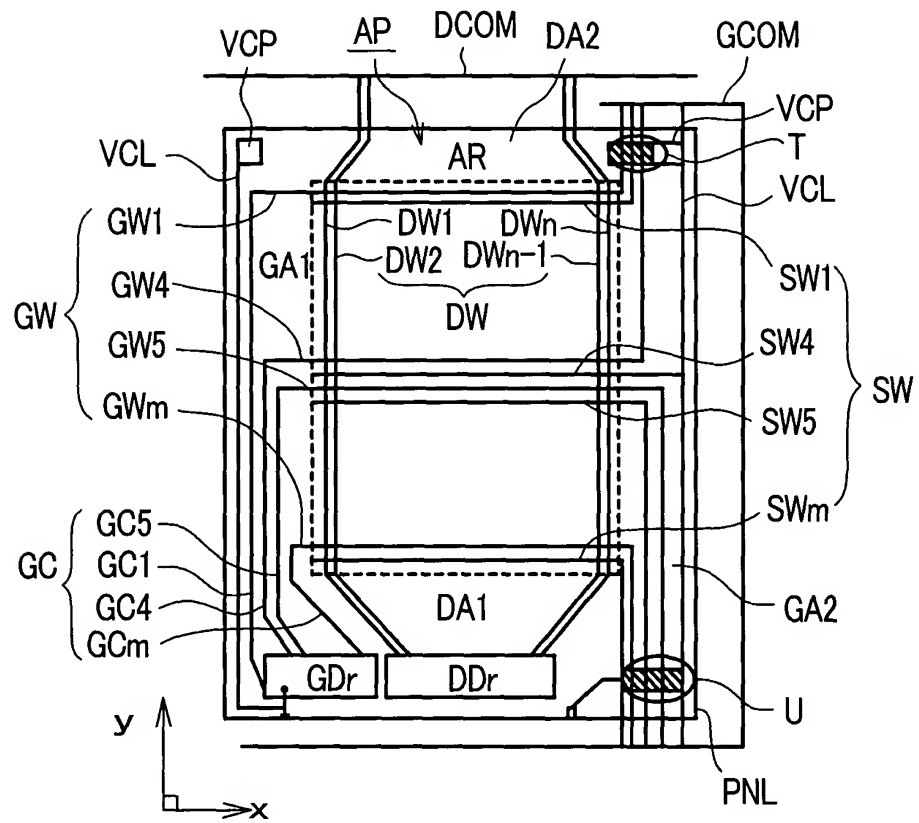


FIG. 10



SW5 1 GW5 4 SW4 GW4 PNL

FIG. 14



The plan view shows a central display area defined by a dashed rectangle. This area is divided into a grid of subpixels by gate wires (GW) and data wires (DA). The gate wires are labeled GW1, GW4, GW5, and GWm. The data wires are labeled DA1 and DA2. The switching elements (SW) are labeled SW1, SW4, SW5, and SWm. The central area is also labeled DW, DW1, DW2, DWn, and DWn-1. The display area is surrounded by a peripheral region (PNL) which contains various components including VCP, VCL, AP, DCOM, GC1, GC4, GC5, GCm, and Dr (GDr, DDr). A coordinate system (x, y) is shown at the bottom left.

FIG. 16

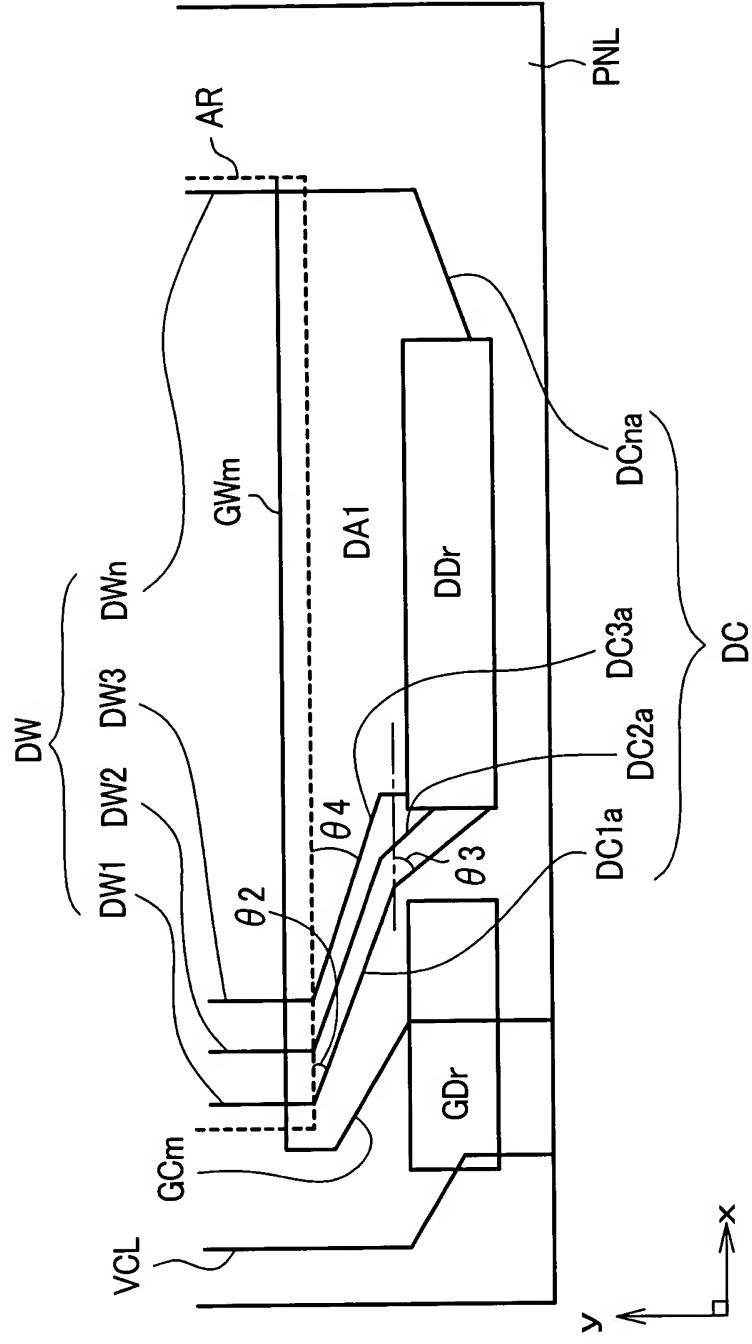


FIG. 17

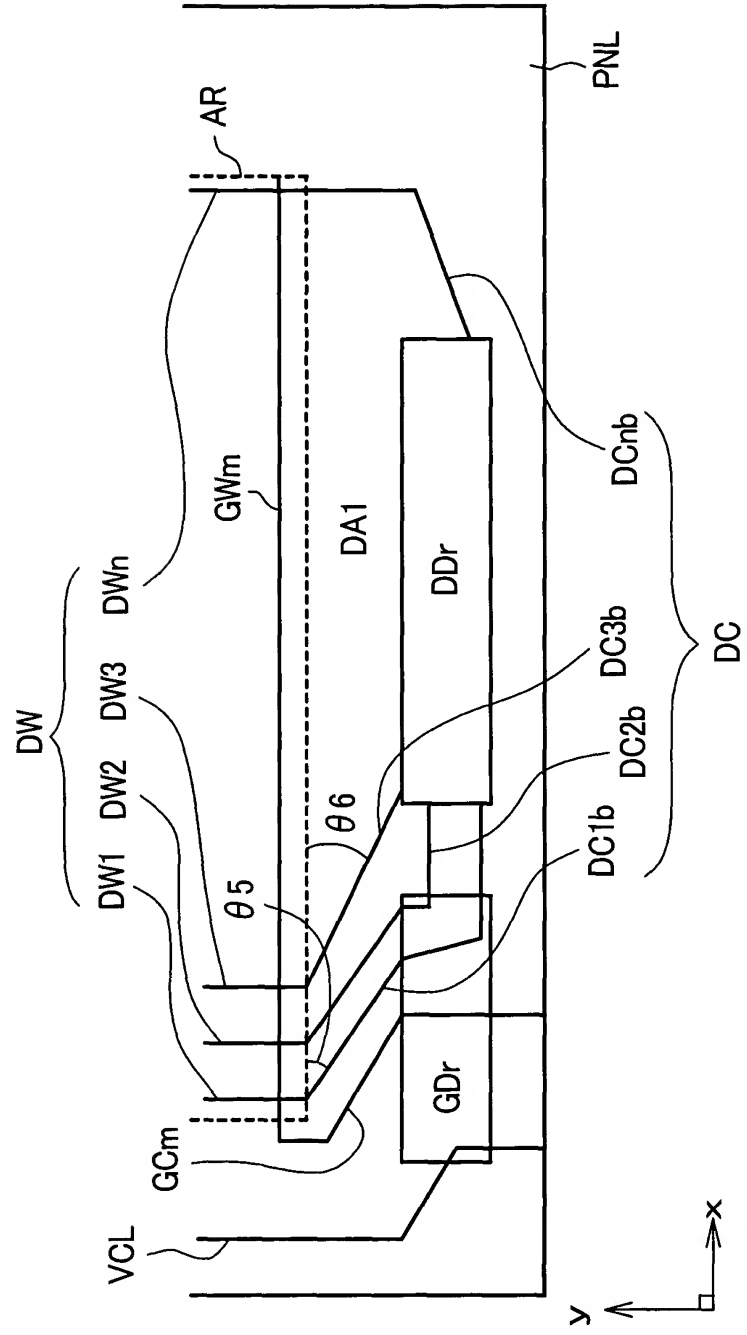


FIG. 18

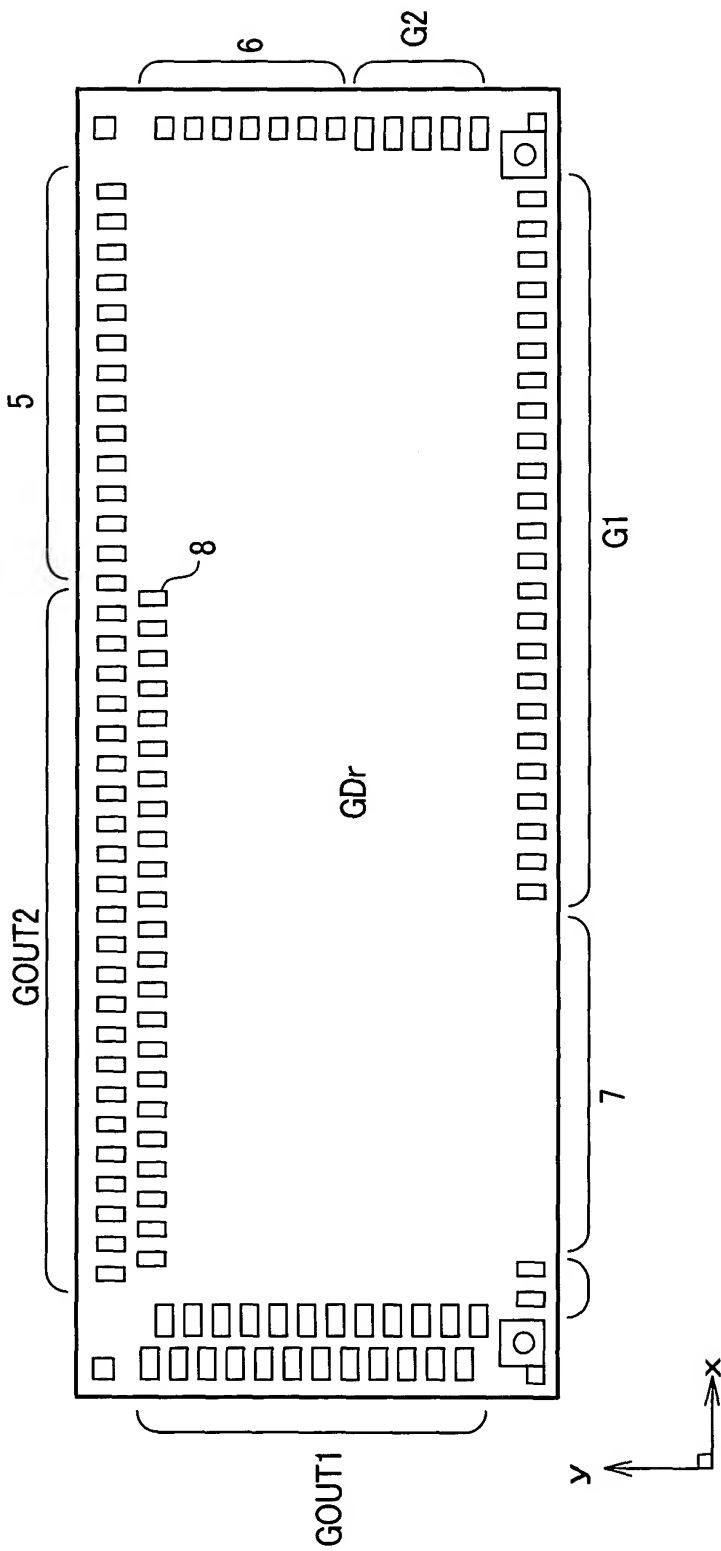


FIG. 19

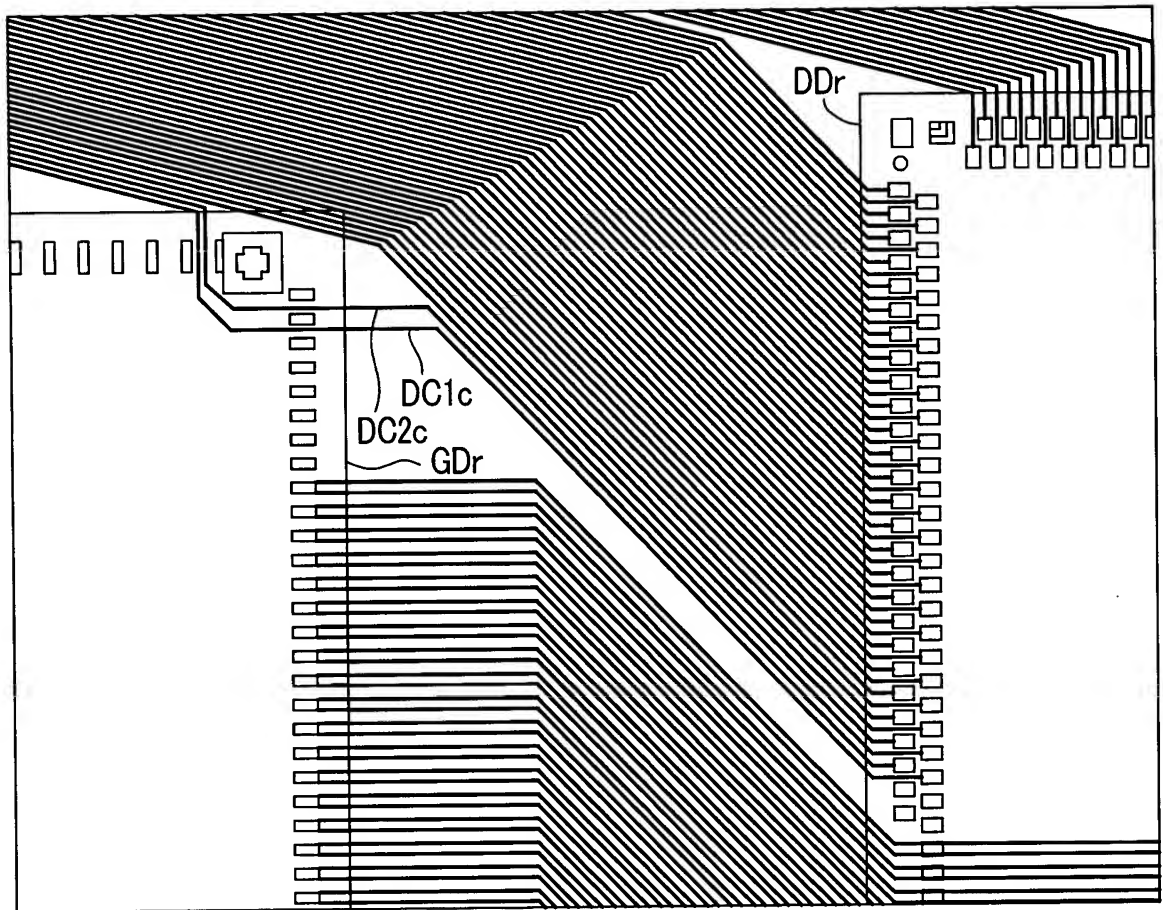


FIG. 20

Prior Art

